DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-2, 11-12, 24, 27-28 and 30-32 are rejected under 35 U.S.C. 102(b) as being anticipated by P.P. Zarrinkar, Genome Research 11:1256-1261, 2001 (herein after Zarrinkar).

For Claim 1, Zarrinkar teaches addition of sample (contacting) to individual arrays of a wafer (common carrier) kept separate by a silicone seal and grid plate (p. 1257, col 1, ¶3; Fig. 1) (multiwell plate) with evaporation prevented by pressing a second seal onto the grid plate (providing closed chamber about each array). Further, Zarrinkar teaches hybridization to the arrays and the steps of the assay following said hybridization (maintaining arrays together with plate) (p. 1257, col 1, ¶ 3-4).

For Claim 2, Zarrinkar teaches arrays use of a single glass wafer (p. 1257, col 1, ¶ 2) (one-piece substrate).

For Claim 11, Zarrinkar teaches a hybridization chamber (housing) for a wafer comprising multiple arrays (p. 1257, col 1, ¶ 3; caption, Fig. 1A and 1B).

For Claim 12, Zarrinkar teaches a plate providing support to the wafer from the back (p. 1257, col 1, ¶ 3) (base) and a solid lid pressing a second seal (p. 1257, col 1, ¶ 3) (from above; a cover).

For Claim 24, Zarrinkar teaches the step of addition (contacting) of sample comprising a hybridization mixture (p. 1257, col 1, ¶ 4) (one or more reagents) to individual arrays of a wafer (set of chemical arrays) kept separate by a silicone seal and grid plate (p. 1257, col 1, ¶3; Fig. 1) (multiwell plate) with evaporation prevented by pressing a second seal onto the grid plate (providing closed chamber about each array). Further, Zarrinkar teaches hybridization to the arrays of the wafer (maintaining arrays together with plate) (p. 1257, col 1, ¶ 3-4).

For Claim 27, Zarrinkar teaches a set of arrays (chemical arrays) arranged on a single wafer (p. 1257, col 1, ¶ 1) (common carrier) and an assembled hybridization chamber (p. 1257, col 1, ¶ 3 and Fig. 1B) (multi-well plate) with a solid lid for preventing hybridization (p. 1257, col 1, ¶ 3) (provide closed chambers about each array).

For Claim 28, Zarrinkar teaches a single glass wafer on which the arrays are disposed (p. 1257, col 1, ¶ 2) (one-piece common carrier).

For Claim 30, Zarrinkar teaches individual arrays of the wafer (common carrier) visible as squares (Fig. 1 and its caption) (indications of locations for separation) and that such wafers are cut into individual arrays (multiple sub-sets with one or more arrays).

For Claim 31, Zarrinkar teaches a hybridization chamber (p. 1257, col 1, ¶ 3 and Fig. 1 with caption) (housing) comprising frame for keeping arrays and samples separate (p. 1257, col 1, ¶ 3) (in an operative configuration) and with a solid lid and second seal onto the grid plate for preventing evaporation (provide closed chambers for each array).

For Claim 32, Zarrinkar teaches a plate providing support to the wafer from the back (p. 1257, col 1, ¶ 3) (base) and a solid lid pressing a second seal onto the grid plate (p. 1257, col 1, ¶ 3) (from above; a cover).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 3-5, 7-8, 13-23, 29 and 33-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over P.P. Zarrinkar, Genome Research 11:1256-1261, 2001 (herein after Zarrinkar).

For Claim 3, Zarrinkar is silent on separating the set of arrays into subsets. Zarrinkar teaches that such wafers comprising multiple arrays are commonly cut into individual arrays (p. 1257, col 1, ¶ 2). Further, Zarrinkar teaches that the assembly comprises a support plate (p. 1257, col 1, ¶ 3); such plate is fully capable of holding sub-sets of the

wafer. One of ordinary skill in the art at the time of the invention would find obvious to apply the teaching of Zarrinkar to use subsets of the entire set in order to accommodate the size requirements of commonly available equipment for post-hybridization washing and scanning.

For Claim 4, Zarrinkar does not teach separation of arrays into subsets along markings. Zarrinkar teaches individual arrays of the wafer (common carrier) visible as squares (Fig. 1 and its caption) (with markings separating arrays) and that such wafers are cut into individual arrays. One of ordinary skill in the art at the time of invention would find obvious to use such markings as guides for separating arrays since such markings provide readily visible landmarks for rapid separation.

For Claim 5, Zarrinkar teaches the wafer (substrate) is glass (p. 1257, col 1, ¶ 2) and that individual arrays are visible (markings present on substrate) as squares. Zarrinkar does not teach that markings comprise scores to facilitate breaking. Rather Zarrinkar teaches that wafers are commonly cut into individual arrays (p. 1257, col 1, ¶ 2). One of ordinary skill in the art at the time of invention would find it obvious to cut along markings as an alternative to breaking along scores in providing a precise and automated means of generating individual sub-sets from wafers (common carrier).

For Claim 6, Zarrinkar does not teach separation of arrays into subsets. Zarrinkar teaches that such wafers comprising multiple arrays are commonly cut before the assay into individual arrays according to Claim 3 above. One of ordinary skill in the art at the time of the invention would find obvious from the teaching of Zarrinkar to separate

arrays after the assay as well as before, in order to allow for efficient processing of the entire array through the steps common to all subsets.

For Claim 7, Zarrinkar teaches the step of using an integrated device (p. 1257, col 1, ¶ 3) (substrate holder) for parallel processing of multiple arrays on a single wafer (p. 1257, col 1, ¶ 1) (substrate). Zarrinkar does not teach sub-sets of arrays mounted at different locations. Zarrinkar does teach that such device can be adapted to other types of arrays, such as those on 1 x 3 in. slides (p. 1257, col 1, ¶ 2). One of ordinary skill in the art at the time of invention would find obvious from the teachings of Zarrinkar that such integrated device could be used for processing subsets of arrays of any size and mounted next to each other, within the size limitation of device, and such arrays could be mounted at different locations and removed (separated) from the device (holder).

For Claim 8, Zarrinkar does not teach mounting of separate substrates in a series. Zarrinkar does teach that such device can be adapted to other arrays, such as those on 1 x 3 in. slides (p. 1257, col 1, ¶ 2). One of ordinary skill in the art at the time of invention would find obvious from the teachings of Zarrinkar to use substrates mounted in any fashion, either in a series and adjacent or out of series, within the limitations of size and dimensions of the device.

For Claim 13, Zarrinkar does not teach the use of a common carrier serving as base or cover. Zarrinkar does teach a solid plate serving as base to prevent breaking of the thin wafer (common carrier). One of ordinary skill in the art at the time of invention would find obvious from the teachings of Zarrinkar to use a carrier of sufficient thickness

and/or durability in order to provide the option of scanning and collecting data from either side of the substrate.

For Claim 14, Zarrinkar does not teach the use of arrays on common carriers of 2n by 3n. Zarrinkar does teach a 7 x 7 arrangement of arrays (p. 1257, col 1, ¶ 1) and that other arrays may be used, including those on 1 x 3 in. slides (p. 1257, col 1, ¶ 2). One of ordinary skill in the art at the time of invention would find obvious from the teachings of Zarrinkar that such carriers may be adapted for use with any arrangement of arrays, within the limitations of spot or feature dimensions and spacing between such spots or features.

For Claim 15, Zarrinkar does not teach the use of arrays on common carriers where n is 4, 8 or 16. One of ordinary skill in the art at the time of invention would find obvious from the teachings of Zarrinkar according to Claim 14 above that such carriers may be adapted for use with any arrangement of arrays, within the limitations of spot or feature dimensions and spacing between such spots or features.

For Claim 16, Zarrinkar does not teach use of a carrier not greater in length and width than 150 mm by 100 mm. Zarrinkar teaches use of a carrier 125 mm by 125 mm (p. 1257, col 1, ¶ 1) and that such wafers are commonly cut into individual arrays (p. 1257, col 1, ¶ 2). One of ordinary skill in the art at the time of invention would find obvious from the teachings of Zarrinkar that such carriers may be adapted for different lengths and widths by removing individual arrays in order to obtain subsets compatible with either the scale of the experiment or the equipment used in processing steps downstream of hybridization.

For Claim 17, Zarrinkar does not teach separating arrays into subsets of the same length and width. Zarrinkar teaches use of wafers comprising 7 by 7 arrays (p. 1257, col 1, ¶ 1) and that wafers are commonly cut into individual arrays (p. 1257, col 1, ¶ 2). One of ordinary skill in the art at the time of invention would find obvious from the teachings of Zarrinkar that such carriers may be cut into sub-sets of any length and width, within the limitations of the original wafer, Including 4 sub-sets of 3 by 3 arrays.

For Claim 18, Zarrinkar does not teach receiving arrays from a remote location. One of ordinary skill in the art at the time of invention would find obvious to receive arrays from a remote location in order to allow for assembly of housing, delivery of samples, hybridizations and additional downstream processing in separate locations. With regard to an indication of locations along which separating occurs, Zarrinkar teaches a wafer of arrays with individual arrays visible as squares (Fig. 1, caption) (markings visible; locations for separating).

For Claim 19, Zarrinkar teaches use of a one-piece substrate that includes multiple arrays (p. 1257, col 1, ¶ 1) (on the surface), and such wafers have markings visible (indication of locations) along which separation occurs (Fig. 1A and 1C and Fig. 1 caption).

For Claim 20, Zarrinkar teaches an use of an assembly (substrate holder) including a support plate (p. 1257, col 1, ¶ 2); said plate is fully capable of holding multiple sub-sets of arrays, each sub-set on its own substrate mounted (at different locations) in the assembly (holder). Further, one of ordinary skill in the art at the time of invention would find obvious that locations at which separate substrates may be removed are visually

indicated, for instance by the edges of the substrates or the interface between adjacent substrates.

For Claim 21, Zarrinkar does not teach reading of separated sub-sets. Zarrinkar teaches scanning (reading) a wafer (p. 1260, col 2, ¶ 2). One of ordinary skill in the art at the time of invention would find obvious to use the capability of the assembly of Zarrinkar, with its support base, to hold/house multiple sub-sets and that such sub-sets would be scanned (read) following separation.

For Claim 22, With regard to receiving a reading result from a remote location, Zarrinkar teaches scanning of wafers with a scanner and digitizing output by an acquisition board in a computer (p. 1260, col 2, ¶ 2) (computer receiving result of reading from a remote location). Such receiving is well known in the art, for instance, when a computer receives data from a slide reader, data transferred on readable medium from one computer to another and data transmitted in data files over an intranet or internet connection.

For Claim 23, With regard to forwarding a result to a remote location, Zarrinkar teaches scanning of wafers by a scanner and digitizing output by an acquisition board in a computer (p. 1260, col 2, ¶ 2) (scanner forwarding result of reading to a remote location).

For Claim 29, Zarrinkar teaches an integrated device (p. 1257, col 1, ¶ 3) (substrate holder) for parallel processing of multiple arrays on a single wafer (p. 1257, col 1, ¶ 1) (substrate). Zarrinkar does not teach multiple sub-sets of arrays. Zarrinkar teaches that such device can be adapted to other types of arrays, such as those on 1 x 3 in. slides

(p. 1257, col 1, ¶ 2). One of ordinary skill in the art at the time of invention would find obvious from the teachings of Zarrinkar that such integrated device (substrate holder) could be used for processing sub-sets of arrays of any size and mounted at different locations on said holder.

For Claim 33, Zarrinkar does not teach the use of a common carrier that serves as base or cover. Zarrinkar does teach a solid plate serving as base to prevent breaking of the thin wafer (common carrier). One of ordinary skill in the art at the time of invention would find obvious from the teachings of Zarrinkar to use a carrier of sufficient thickness and/or durability, and without a base, in order to provide the option of scanning and collecting data from either side of the substrate.

For Claim 34, Zarrinkar teaches a set of arrays (chemical arrays) on a glass wafer (p. 1257, col 1, ¶ 1) (common carrier) with samples added to the arrays (p. 1257, col 1, ¶ 3) (arrays previously exposed to sample). , Zarrinkar does not teach separating the set of arrays into multiple sub-sets. Zarrinkar does teach that wafers are commonly separated into individual arrays (p. 1257, col 1, ¶ 2). Further, Zarrinkar teaches the wafer (substrate) is glass (p. 1257, col 1, ¶ 2) that individual arrays are visible as squares (markings present on substrate). Zarrinkar does not teach that markings are scores to facilitate breaking, rather that wafers are commonly cut into individual arrays (p. 1257, col 1, ¶ 2). One of ordinary skill in the art at the time of invention would find obvious to use cutting along markings as an alternative to breaking along scores in providing a precise and automated means of generating individual sub-sets from wafers (common carrier).

For Claim 35, Zarrinkar does not teach the step of receiving a set of arrays from a remote location. Zarrinkar does teach markings on the wafer (common carrier) along which separation of arrays occurs (Fig. 1 and caption). One of ordinary skill in the art at the time of invention would find obvious to use receipt of arrays from a remote location to provide the option of addition of reagents to hybridization chambers, possibly containing PCR products, in a location remote from that used for hybridization and subsequent processing, in order to minimize the contamination of clean areas with PCR products, or in order to accommodate the space needs of separate pieces of equipment in processing such arrays.

For Claim 36, Zarrinkar does not teach a kit of the claimed components. However, Zarrinkar does teach the components of said kit including a set of arrays (chemical arrays) arranged on a single wafer (p. 1257, col 1, ¶ 1) (common carrier) and an assembled hybridization chamber (p. 1257, col 1, ¶ 3 and Fig. 1B) (multiwell plate) with a solid lid for preventing hybridization (p. 1257, col 1, ¶ 3) (provide closed chambers about each array).

For Claim 37, Zarrinkar teaches a hybridization chamber (p. 1257, col 1, ¶ 3 and Fig. 1 with caption) (housing) comprising frame and grid with seal for keeping arrays and samples separate (p. 1257, col 1, ¶ 3) (maintaining arrays in an operative configuration) and with a solid lid and second seal onto the grid plate for preventing evaporation (provide closed chambers for each array).

For Claim 38, Zarrinkar teaches a plate providing support to the wafer from the back (p. 1257, col 1, ¶ 3) (base) and a solid lid pressing a second seal onto the grid plate (p. 1257, col 1, ¶ 3) (from above; a cover).

For Claim 39, Zarrinkar teaches a sample (comprises at least one reagent) is added to each array (well of hybridization chamber/multiwell plate) for implementing a hybridization (p. 1257, col 1, ¶ 3) (chemical reaction). One of ordinary skill in the art at the time of invention would find obvious to use the components of Zarrinkar in assembling a kit since such kits provide convenient availability of required components from a single source.

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrinkar as applied to claim 3 above, and further in view of P.J. Muraca, U.S. Patent Application Publication 20020168639 (herein after Muraca).

For Claim 9, Zarrinkar does not teach multiple array identifiers. Muraca teaches identifiers present on the array substrate ([0144]). One of ordinary skill in the art at the time of invention would find obvious to use such identifiers in order to retain an association of each sample with its own array before and after separation.

For Claim 10, Zarrinkar does not teach retrieving array layout information from array identifiers. Muraca teaches identifiers on array substrate comprising information including identity and address of sublocations on the array (array layout information) ([0144]). One of ordinary skill in the art at the time of invention would find obvious to use

such identifiers in order to retain an association of array with its annotation, essential for interpreting expression.

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrinkar as applied to Claim 24 above, and further in view of P. Heaney et al. US Patent Application Publication 20040029258 (herein after Heaney).
For Claim 25, Zarrinkar is silent on use of an amplification reaction in the multiwell plate. Heaney teaches a containment member (closed chamber) removably attached to a substrate to form a chamber for biochemical processes including thermal cycling of material (abstract) (amplification reaction), one embodiment of which comprises capture of an amplification product by an oligonucleotides immobilized on the substrate ([0290]). One of ordinary skill in the art at the time of invention would find obvious to use the substrate and chamber of Heaney in order to provide a convenient way to capture PCR products on the substrate, thereby increasing the sensitivity of an assay by increasing the concentration of product in a confined area.

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrinkar in further view of M. Matzke et al., Genetics 158:451-461, May 2001.
For Claim 26, Zarrinkar does not teach the step of cellular transvection reaction. Matzke teaches that transvection involves activation of gene expression *in trans* and that cell lines can be used for measurements of the effects of transvection events (abstract). One of ordinary skill in the art at the time of invention would find obvious to use the

teachings of Matzke with the substrate of Zarrinkar, to measure the effects of gene transcription following cell lysis and capture of transcripts on probes bound to the substrate, in order to obtain a convenient and one step and high throughput assay for such assays.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. R.P. Rava et al., U.S. Patent 5,545,531, R.R. Rava et al., U.S. Patent 5,874,219, S. C. Dahm et al., U.S. Patent 6,399,394, A.A. Jacobs et al., U.S. Patent Application Publication 200200950783, E.J. Spence, U.S. Patent Application Publication 20030157700.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIMOTHY G. KINGAN whose telephone number is (571)270-3720. The examiner can normally be reached on Monday-Friday, 8:30 A.M. to 5:00 P.M., E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jill Warden can be reached at 571-272-1267. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TGK

/Jill Warden/
Supervisory Patent Examiner, Art Unit 1797